REDUNDANT SINGLE EVENT UPSET SUPRESSION SYSTEM

ABSTRACT

CMOS transistors are configured to operate as either a redundant, SEU-tolerant, positive-logic, cross-coupled Nor Gate SR-flip flop or a redundant, SEU-tolerant, negative-logic, cross-coupled Nand Gate SR-flip flop. The register can operate as a memory, and further as a memory that can overcome the effects of radiation. As an SR-flip flop, the invention can be altered into any known type of latch or flip-flop by the application of external logic, thereby extending radiation tolerance to devices previously incapable of radiation tolerance. Numerous registers can be logically connected and replicated thereby being electronically configured to operate as a redundant circuit.